What is claimed is:

1. A semiconductor device comprising:

a non-volatile memory element including a first source electrode, a first drain electrode, a floating gate electrode and a control gate electrode, and capable of having different threshold voltages;

a read transistor element including a second source electrode, a second drain electrode and the floating gate electrode as a gate electrode, and capable of having different mutual conductances according to the threshold voltage of the non-volatile memory element; and

transmission means of a signal generated according to the mutual conductance of the read transistor element.

2. A semiconductor device according to claim 1, wherein the ground voltage of a circuit is applied to the first source electrode and the first drain electrode in a read operation.

3. A semiconductor device according to claim 1 or claim 2, wherein the read transistor element is a depression type MIS transistor and the control gate electrode is set at a non-select level in a read operation.

4. A semiconductor device according to any one of

claims 1 to 3, wherein the read transistor element is an enhancement type MIS transistor and the control gate electrode is set at a select level in a read operation.

5. A semiconductor device according to claim 1, wherein the non-volatile memory element includes a MIS capacitor element having a capacitor electrode on a first semiconductor region functioning as a control gate electrode via an insulating layer and a MIS transistor including a first source electrode, a first drain electrode and a gate electrode which are formed on a second semiconductor region, the capacitor electrode being connected to the gate electrode and functioning as a floating gate electrode.

6. A semiconductor device according to claim 1, wherein the non-volatile memory element includes; a first conductivity type first well region formed on a semiconductor substrate; a second conductivity type second well region formed on the semiconductor substrate; a second conductivity type first source electrode region which is formed on the first well region and is to be connected to a first signal line; a second conductivity type first drain electrode region which is formed on the first well region and is to be connected to a second signal line; a first

insulating film formed on the principal surface of the first well region at the position between the first source electrode region and the first drain electrode region; a second insulating film formed on the principal surface of the second well region; a floating gate electrode region formed on the first and second insulating films; and a control gate electrode region which is formed on the second well region and is to be connected to a third signal line.

7. A semiconductor device according to claim 1, wherein the non-volatile memory element is provided in a pair and the read transistor element is provided in a pair, wherein the floating gate electrode of one of the non-volatile memory elements is shared by one of the read transistor elements and the floating gate electrode of the other non-volatile memory element is shared by the other read transistor element, and wherein the pair of read transistor elements are connected in parallel to the transmission means.

8. A semiconductor device according to claim 1, wherein the non-volatile memory element is provided in a pair and the read transistor element is provided in a pair, wherein the floating gate electrode of one of the non-volatile memory elements is shared by one of the read transistor elements and the floating gate

electrode of the other non-volatile memory element is shared by the other read transistor element, and wherein the pair of read transistor elements are connected in series to the transmission means.

9. A semiconductor device according to claim 8, further comprising a plurality of unit information cells, each of which is composed of the pair of non-volatile memory elements and the pair of read transistor elements, and an electric program circuit to the non-volatile memory elements of the plurality of unit information cells, wherein the plurality of unit information cells are made the memory circuit of recovery information to a circuit to be recovered.

10. A semiconductor device according to claim 9, further comprising a fuse program circuit for memorizing recovery information according to the melting state of a fuse element as another recovery information memory circuit to the circuit to be recovered.

11. A semiconductor device according to claim 9, wherein the circuit to be recovered is the memory cell array in which a DRAM is built.

12. A semiconductor device according to claim 9, wherein the circuit to be recovered is the memory cell array of a DRAM in which a microcomputer is built.

13. A semiconductor device according to claim 9, wherein the circuit to be recovered is the memory cell array of an SRAM in which a microcomputer is built.

14. A semiconductor device according to claim 13, wherein the electric program circuit has an operation mode of prohibiting writing into the unit information cell, when an ECC circuit is effective.

15. A semiconductor device according to claim 8, further comprising a plurality of unit information cells each of which is composed of the pair of non-volatile memory cells and the pair of read transistor elements, wherein a part of the plurality of unit information cells are made a region for holding an error correction code to the memory information of the remaining unit information cells, an electric program circuit to the non-volatile memory elements of the plurality of unit information cells, and an ECC circuit capable of making an error correction to the read information of the plurality of unit information cells.

16. A semiconductor device comprising:

a non-volatile memory element including a first source electrode, a first drain electrode, a floating gate electrode and a control gate electrode, and capable of having different threshold voltages;

a read transistor element including a second source electrode, a second drain electrode and the floating gate electrode as a gate electrode, and capable of having different switching states according to the threshold voltage of the non-volatile memory element; and

transmission circuit of a signal generated according to the switching state of the read transistor element.

17. A semiconductor device according to claim 16, wherein the ground voltage of a circuit is applied to the first source electrode and the first drain electrode in a read operation.

18. A semiconductor device according to claim 16, wherein the read transistor element is a depression type MIS transistor and the control gate electrode is set at a non-select level in a read operation.

19. A semiconductor device according to claim 16, wherein the read transistor element is an enhancement type MIS transistor and the control gate electrode is set at a select level in a read operation.

20. A semiconductor device according to claim 16, wherein the non-volatile memory element includes a MIS capacitor element having a capacitor electrode formed on a first semiconductor region functioning as a

control gate electrode via an insulating layer and a MIS transistor including a first source electrode, a first drain electrode and a gate electrode which are formed on a second semiconductor region, the capacitor electrode being connected to the gate electrode and functioning as a floating gate electrode.

21. A semiconductor device according to claim 16, wherein the non-volatile memory element includes; a first conductivity type first well region formed on a semiconductor substrate; a second conductivity type second well region formed on the semiconductor substrate; a second conductivity type first source electrode region which is formed on the first well region and is to be connected to a first signal line; a second conductivity type first drain electrode region which is formed on the first well region and is to be connected to a second signal line; a first insulating film formed on the principal surface of the first well region at the position between the first source electrode region and the first drain electrode region; a second insulating film formed on the principal surface of the second well region; a floating gate electrode region formed on the first and second insulating films; and a control gate electrode region which is formed on the second well region and

is to be connected to a third signal line.

22. A semiconductor device according to claim 16, wherein the non-volatile memory element is provided in a pair and the read transistor element is provided in a pair, wherein the floating gate electrode of one of the non-volatile memory elements is shared by one of the read transistor elements and the floating gate electrode of the other non-volatile memory element is shared by the other read transistor element, and wherein the pair of read transistor elements are connected in parallel to the transmission means.

23. A semiconductor device claim 16, wherein the non-volatile memory element is provided in a pair and the read transistor element is provided in a pair, wherein the floating gate electrode of one of the non-volatile memory elements is shared by one of the read transistor elements and the floating gate electrode of the other non-volatile memory element is shared by the other read transistor element , and wherein the pair of read transistor elements are connected in series to the transmission means.

24. A semiconductor device according to claim 23, further comprising a plurality of unit information cells, each of which is composed of the pair of non-volatile memory elements and the pair of read

transistor elements, and an electric program circuit to the non-volatile memory elements of the plurality of unit information cells, wherein the plurality of unit information cells are made the memory circuit of recovery information to a circuit to be recovered.

25. A semiconductor device according to claim 23, further comprising a fuse program circuit for memorizing recovery information according to the melting state of a fuse element as another recovery information memory circuit to the circuit to be recovered.

26. A semiconductor device according to claim 23, wherein the circuit to be recovered is the memory cell array in which a DRAM is built.

27. A semiconductor device according to claim 23, wherein the circuit to be recovered is the memory cell array of a DRAM in which a microcomputer is built.

28. A semiconductor device according to claim 23, wherein the circuit to be recovered is the memory cell array of an SRAM in which a microcomputer is built.

29. A semiconductor device according to claim 28, wherein the electric program circuit has an operation mode of prohibiting writing into the unit information cell, when an ECC circuit is effective.

30. A semiconductor device according to claim 16,

further comprising a plurality of unit information cells each of which is composed of the pair of non-volatile memory cells and the pair of read transistor elements, wherein a part of the plurality of unit information cells are made a region for holding an error correction code to the memory information of the remaining unit information cells, an electric program circuit to the non-volatile memory elements of the plurality of unit information cells, and an ECC circuit capable of making an error correction to the read information of the plurality of unit information cells.

31. A semiconductor device comprising:

a non-volatile memory element including a first source electrode, a first drain electrode, a floating gate electrode and a control gate electrode, and capable of having different threshold voltages;

a read transistor element including a second source electrode, a second drain electrode and the floating gate electrode as a gate electrode, and capable of having different threshold voltages according to the threshold voltage of the non-volatile memory element; and

transmission circuit of a signal generated according to the threshold voltage of the read

transistor element.

32. A semiconductor device according to claim 31, wherein the ground voltage of a circuit is applied to the first source electrode and the first drain electrode in a read operation.

33. A semiconductor device according to claim 31, wherein the read transistor element is a depression type MIS transistor and the control gate electrode is set at a non-select level in a read operation.

34. A semiconductor device according to claim 31, wherein the read transistor element is an enhancement type MIS transistor and the control gate electrode is set at a select level in a read operation.

35. A semiconductor device according to claim 31, wherein the non-volatile memory element includes a MIS capacitor element having a capacitor electrode on a first semiconductor region functioning as a control gate electrode via an insulating layer and a MIS transistor including a first source electrode, a first drain electrode and a gate electrode which are formed on a second semiconductor region, the capacitor electrode being connected to the gate electrode and functioning as a floating gate electrode.

36. A semiconductor device according to claim 31, wherein the non-volatile memory element includes; a

first conductivity type first well region formed on a semiconductor substrate; a second conductivity type second well region formed on the semiconductor substrate; a second conductivity type first source electrode region which is formed on the first well region and is to be connected to a first signal line; a second conductivity type first drain electrode region which is formed on the first well region and is to be connected to a second signal line; a first insulating film formed on the principal surface of the first well region at the position between the first source electrode region and the first drain electrode region; a second insulating film formed on the principal surface of the second well region; a floating gate electrode region formed on the first and second insulating films; and a control gate electrode region which is formed on the second well region and is to be connected to a third signal line.

37. A semiconductor device according to claim 31, wherein the non-volatile memory element is provided in a pair and the read transistor element is provided in a pair, wherein the floating gate electrode of one of the non-volatile memory elements is shared by one of the read transistor elements and the floating gate electrode of the other non-volatile memory element is

shared by the other read transistor element, and wherein the pair of read transistor elements are connected in parallel to the transmission means.

38. A semiconductor device according to claim 31, wherein the non-volatile memory element is provided in a pair and the read transistor element is provided in a pair, wherein the floating gate electrode of one of the non-volatile memory elements is shared by one of the read transistor elements and the floating gate electrode of the other non-volatile memory element is shared by the other read transistor element, and wherein the pair of read transistor elements are connected in series to the transmission means.

39. A semiconductor device according to claim 38, further comprising a plurality of unit information cells, each of which is composed of the pair of non-volatile memory elements and the pair of read transistor elements, and an electric program circuit to the non-volatile memory elements of the plurality of unit information cells, wherein the plurality of unit information cells are made the memory circuit of recovery information to a circuit to be recovered.

40. A semiconductor device according to claim 38, further comprising a fuse program circuit for memorizing recovery information according to the

melting state of a fuse element as another recovery information memory circuit to the circuit to be recovered.

41. A semiconductor device according to claim 38, wherein the circuit to be recovered is the memory cell array in which a DRAM is built.

42. A semiconductor device according to claim 38, wherein the circuit to be recovered is the memory cell array of a DRAM in which a microcomputer is built.

43. A semiconductor device according to claim 38, wherein the circuit to be recovered is the memory cell array of an SRAM in which a microcomputer is built.

44. A semiconductor device according to claim 43, wherein the electric program circuit has an operation mode of prohibiting writing into the unit information cell, when an ECC circuit is effective.

45. A semiconductor device according to claim 31, further comprising a plurality of unit information cells each of which is composed of the pair of non-volatile memory cells and the pair of read transistor elements, wherein a part of the plurality of unit information cells are made a region for holding an error correction code to the memory information of the remaining unit information cells, an electric program circuit to the non-volatile memory elements of the

plurality of unit information cells, and an ECC circuit capable of making an error correction to the read information of the plurality of unit information cells.